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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,358	01/21/2004	Naoki Yamamoto	501.38505CX2	8710

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EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,358	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-13 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-6 of copending Application No. 10/821,842. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: heat treating a semiconductor in a hydrogen/water vapor or moisture atmosphere.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,482,740 to Soininen et al.

In regards to claim 1, Soininen teaches a process for manufacturing a semiconductor integrated circuit device, which comprises the steps of: (a) forming, over the silicon surface on a main surface of a wafer, an insulating film having an effective film thickness less than 5 nm in terms of SiO_2 and made of a single insulating film containing silicon oxide as a principal component or a composite film thereof with another insulating film; (b) forming, over the insulating film, a metal film containing a refractory metal as a principal component without disposing, therebetween, an intermediate layer containing polycrystalline silicon as a principal component; (c) heat treating the wafer in a water-vapor- and hydrogen-containing gas atmosphere having a water vapor/hydrogen partial pressure ratio set at a ratio permitting oxidation of silicon without substantial oxidation of the refractory metal; and (d) after step (c), patterning the metal film to form a metal gate electrode at column 6, lines 55-67.

In regards to claim 2, Soininen teaches the process according to claim 1, wherein the refractory metal is molybdenum or tungsten at column 6, lines 1-3.

In regards to claim 3, Soininen teaches a processing according to claim 1 , wherein the insulating film has an effective film thickness less than 4 nm in terms of SiO_2 at column 5, lines 45-47.

In regards to claim 4, Soininen teaches a process according to claim 1, wherein the insulating film has an effective film thickness less than 3 nm in terms of SiO_2 at column 5, lines 45-50.

In regards to claim 5, Soininen teaches a process for manufacturing a semiconductor integrated circuit device, which comprises the steps of: (a) forming, over the silicon surface on a main surface of a wafer, an insulating film having an effective film thickness less than 5 nm in terms of SiO_2 and made of a single insulating film containing silicon nitride as a principal component or a composite film thereof with another insulating film; (b) forming, over the insulating film, a metal film containing a refractory metal as a principal component without disposing, therebetween, an intermediate layer containing polycrystalline silicon as a principal component', (c) heat treating the wafer in a water-vapor- and hydrogen-containing gas atmosphere having a water vapor/hydrogen partial pressure ratio set at a ratio permitting oxidation of silicon without substantial oxidation of the refractory metal; and (d) after step (c), patterning the metal film to form a metal gate electrode at column 6, lines 55-67.

In regards to claim 6, Soininen teaches a process according to claim 5, wherein the refractory metal is molybdenum or tungsten at column 6, lines 1-3.

In regards to claim 7, teaches a process according to claim 5, wherein the water-vapor and hydrogen-containing gas further contains a nitrogen or ammonia gas at column 11, line 35.

In regards to claim 8, Soininen teaches a process for manufacturing a semiconductor integrated circuit device, which comprises the steps of: (a) forming, over the silicon surface on a main surface of a wafer, an insulating film having an effective film thickness less than 5 nm in terms of SiO_2 and made of a single insulating film containing as a principal component a metal oxide having a dielectric constant larger than silicon dioxide or a composite film thereof with another insulating film; (b) forming, over the insulating film, a metal film containing a refractory metal as a principal component without disposing, therebetween, an intermediate layer containing polycrystalline silicon as a principal component; (c) heat treating the wafer in a water-vapor- and hydrogen-containing gas atmosphere having a water vapor/hydrogen partial pressure ratio set at a ratio permitting oxidation of the material of the insulating film without substantial oxidation of the refractory metal; and (d) after step (c), patterning the metal film to form a metal gate electrode at column 6, lines 55-67.

In regards to claim 9, Soininen teaches a process according to claim 8, wherein the metal constituting the metal oxide film at column 6, lines 44-54.

In regards to claim 10, Soininen teaches a process according to claim 8, wherein the metal constituting the metal oxide film at column 6, lines 44-54.

In regards to claim 11, Soininen teaches a process according to claim 8. wherein the metal constituting the metal oxide film at column 6, lines 44-56.

In regards to claim 12, Soininen teaches a process according to claim 8, wherein the metal oxide film is a high dielectric substance including a ABO_3 type average perovskite structure and is in a paraelectric phase at an operating temperature at column 5, lines 56-57.

In regards to claim 13, Soininen teaches a process according to claim 12, wherein the high dielectric substance is barium strontium titanate at column 5, line 57.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (703) 305-4544. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nelms
Supervisory Patent Examiner
Technology Center 2800

RRB

September 20, 2004